IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An electronic device comprising:

a source signal line driver circuit;

a first gate signal line driver circuit;

a second gate signal line driver circuit; and

a pixel portion including a plurality of pixels,

wherein at least one of said plurality of pixels ~~each have~~ has an EL element, an EL driving TFT for controlling luminescence of ~~each of~~ the EL ~~elements~~ element, a switching TFT, and an eliminating TFT for controlling said EL driving TFT,

wherein said switching TFT is controlled by said first gate signal line driver circuit,

wherein said eliminating TFT is controlled by said second gate signal line driver circuit, and

wherein a gray-scale display is performed by controlling a luminescing time of said plurality of EL elements.

2. (Currently Amended) A device according to claim 1, wherein each of said switching TFT, the EL driving TFT, and the eliminating TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

3. (Currently Amended) A device according to claim 1, wherein said EL driving TFT becomes an OFF state when an electric potential of ~~said~~ a power supply line is applied to ~~said~~ a gate electrode of said EL driving TFT.

4. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 1.

5. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 1.

6. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 1.

7. (Currently Amended) An electronic device comprising:

a source signal line driver circuit electrically connected to a plurality of source signal lines;

a first gate signal line driver circuit electrically connected to a plurality of first gate signal lines;

a second gate signal line driver circuit electrically connected to a plurality of second gate signal lines;

a pixel portion including a plurality of pixels; and

a plurality of power supply ~~line~~ lines,

wherein at least one of said plurality of pixels ~~each have~~ has a ~~switching~~ first TFT, ~~an EL driving~~ a second TFT, ~~an eliminating~~ a third TFT, and an EL element,

wherein a gate electrode of said ~~switching~~ first TFT is electrically connected to one of said plurality of first gate signal ~~line~~ lines,

wherein one of a source region and a drain region of said ~~switching~~ first TFT is electrically connected to one of said plurality of source signal lines, and ~~another~~ the other ~~thereof~~ of the source

region and the drain region of the first TFT is electrically connected to a gate electrode of said ~~EL driving~~ second TFT,

wherein a gate electrode of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of second gate signal ~~line~~ lines,

wherein one of a source region and a drain region of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of power supply ~~line~~ lines, and ~~another~~ the other ~~thereof~~ of the source region and the drain region of the third TFT is electrically connected to said gate electrode of said ~~EL driving~~ second TFT, and

wherein one of a source region and a drain region of said ~~EL driving~~ second TFT is electrically connected to the one of said plurality of power supply ~~line~~ lines, and ~~another~~ the other of the source region and the drain region of the third TFT is electrically connected to said EL element.

8. (Currently Amended) A device according to claim 7, wherein each of said ~~switching~~ first TFT, the ~~EL driving~~ second TFT, and the ~~eliminating~~ third TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

9. (Currently Amended) A device according to claim 7, wherein said ~~EL driving~~ second TFT becomes an OFF state when an electric potential of the one of said plurality of power supply ~~line~~ lines is applied to said gate electrode of said ~~EL driving~~ second TFT.

10. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 7.

11. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 7.

12. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 7.

13. (Currently Amended) An electronic device comprising:

a source signal line driver circuit electrically connected to a plurality of source signal lines;

a first gate signal line driver circuit electrically connected to a plurality of first gate signal lines;

a second gate signal line driver circuit electrically connected to a plurality of second gate signal lines;

a pixel portion including a plurality of pixels; and

a plurality of power supply ~~line~~ lines ~~held at a constant electric potential~~,

wherein at least one of said plurality of pixels ~~each have~~ has a ~~switching~~ first TFT, ~~an EL driving~~ a second TFT, ~~an eliminating~~ a third TFT and an EL element;

wherein said EL element includes a pixel electrode, an opposing electrode ~~held at a constant electric potential~~, and an EL layer formed between said pixel electrode and said opposing electrode,

wherein a gate electrode of said ~~switching~~ first TFT is electrically connected to one of said plurality of first gate signal lines,

wherein one of a source region and a drain region of said ~~switching~~ first TFT is electrically connected to one of said plurality of source signal lines, and ~~another~~ the other ~~thereof~~ of the source region and the drain region of the first TFT is electrically connected to a gate electrode of said ~~EL driving~~ second TFT,

wherein a gate electrode of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of second gate signal lines,

wherein one of a source region and a drain region of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of power supply ~~line~~ lines, and ~~another~~ the other of the source region and the drain region of the third TFT is electrically connected to [[a]] the gate electrode of said ~~EL driving~~ second TFT, and

wherein one of a source region and a drain region of said ~~EL driving~~ second TFT is electrically connected to the one of said plurality of power supply ~~line~~ lines, and ~~another~~ the other of the source region and the drain region of the second TFT is electrically connected to [[a]] the pixel electrode of said EL element.

14. (Currently Amended) A device according to claim 13, wherein said EL layer [[is]] comprises a low molecular organic material or a polymer organic material.

15. (Currently Amended) A device according to claim 14, wherein said low molecular organic material ~~is made of~~ comprises at least one of Alq_3 (tris-8-quinolilite-aluminum) [[or]] and TPD (triphenylamine derivative).

16. (Currently Amended) A device according to claim 14, wherein said polymer organic material ~~is made of~~ comprises at least one of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), [[or]] and polycarbonate.

17. (Currently Amended) A device according to claim 13, wherein each of said ~~switching~~ first TFT, the ~~EL driving~~ second TFT, and the ~~eliminating~~ third TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

18. (Currently Amended) A device according to claim 13, wherein said ~~EL driving~~ second TFT becomes an OFF state when an electric potential of the one of said plurality of power supply ~~line~~ lines is applied to said gate electrode of said ~~EL driving~~ second TFT.

19. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according claim 13.

20. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according claim 13.

21. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 13.

22. (Currently Amended) An electronic device comprising:

a source signal line driver circuit [[,]] ;

a first gate signal line driver circuit [[,]] ;

a second gate signal line driver circuit [[,]] ;

a pixel portion including a plurality of pixels [[,]] ;

a plurality of source signal lines electrically connected to said source signal line driver circuit [[,]] ;

a plurality of first gate signal lines electrically connected to said first gate signal line driver circuit [[,]] ;

a plurality of second gate signal lines electrically connected to said second gate signal line driver circuit [[,]] ; and

a plurality of power supply ~~line~~ lines,

wherein:

at least one of said plurality of pixels ~~each have~~ has a ~~switching~~ first TFT, ~~an EL driving~~ a second TFT, ~~an eliminating~~ a third TFT, and an EL element;

a gate electrode of said ~~switching~~ first TFT is electrically connected to one of said plurality of first gate signal lines;

one of a source region and a drain region of said ~~switching~~ first TFT is electrically connected to one of said plurality of source signal lines, and ~~another thereof~~ the other of the source region and the drain region of the first TFT is electrically connected to a gate electrode of said ~~EL driving~~ second TFT;

a gate electrode of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of second gate signal lines;

one of a source region and a drain region of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the third TFT is electrically connected [[a]] the gate electrode of said ~~EL driving~~ second TFT;

one of a source region and a drain region of said ~~EL driving~~ second TFT is electrically connected to the one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the second TFT is electrically connected to said EL element;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said entire plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1);

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same; and

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$.

23. (Original) A device according to claim 22, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

24. (Original) A device according to claim 22, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

25. (Currently Amended) A device according to claim 22, wherein each of said ~~switching~~ first TFT, the ~~EL driving~~ second TFT, and the ~~eliminating~~ third TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

26. (Currently Amended) A device according to claim 22, wherein said ~~EL driving~~ second TFT becomes an OFF state when an electric potential of the one of said plurality of power supply ~~line~~ lines is applied to said gate electrode of said ~~EL driving~~ second TFT.

27. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 22.

28. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 22.

29. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 22.

30. (Currently Amended) An electronic device comprising :

a source signal line driver circuit [[,]] ;

a first gate signal line driver circuit [[,]] ;

a second gate signal line driver circuit [[,]] ;

a pixel portion including a plurality of pixels [[,]] ;

a plurality of source signal lines electrically connected to said source signal line driver circuit [[,]] ;

a plurality of first gate signal lines electrically connected to said first gate signal line driver circuit [[,]] ;

a plurality of second gate signal lines electrically connected to said second gate signal line driver circuit [[,]] ; and

a plurality of power supply lines ~~line held at a constant electric potential~~,

wherein:

at least one of said plurality of pixels ~~each have~~ has a ~~switching~~ first TFT, ~~an EL driving~~ a second TFT, ~~an eliminating~~ a third TFT and an EL element;

said EL element includes a pixel electrode, an opposing electrode ~~held at a constant electric potential~~, and an EL layer formed between said pixel electrode and said opposing electrode;

a gate electrode of said ~~switching~~ first TFT is electrically connected to one of said plurality of first gate signal lines;

one of a source region and a drain region of said ~~switching~~ first TFT is electrically connected to one of said plurality of source signal lines, ~~another thereof~~ the other of the source region and the drain region of the first TFT is electrically connected to a gate electrode of said ~~EL driving~~ second TFT;

a gate electrode of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of second gate signal lines,

one of a source region and a drain region of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the third TFT is electrically connected to [[a]] the gate electrode of said ~~EL driving~~ second TFT;

one of a source region and a drain region of said ~~EL driving~~ second TFT is electrically connected to the one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the second TFT is electrically connected to [[a]] the pixel electrode of said EL element;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1),

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same; and

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$.

31. (Original) A device according to claim 30, wherein said EL layer is a low molecular organic material or a polymer organic material.

32. (Currently Amended) A device according to claim 30, wherein said low molecular organic material ~~is made of~~ comprises at least one of Alq_3 (tris-8-quinolilite-aluminum) [[or]] and TPD (triphenylamine derivative).

33. (Currently Amended) A device according to claim 30, wherein said polymer organic material ~~is made of~~ comprises at least one of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), [[or]] and polycarbonate.

34. (Original) A device according to claim 30, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

35. (Original) A device according to claim 30, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

36. (Currently Amended) A device according to claim 30, wherein each of said ~~switching~~ first TFT, the ~~EL driving~~ second TFT, and the ~~eliminating~~ third TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

37. (Currently Amended) A device according to claim 30, wherein said ~~EL driving~~ second TFT becomes an OFF state when an electric potential of the one of said plurality of power supply ~~line~~ lines is applied to said gate electrode of said ~~EL driving~~ second TFT.

38. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 30.

39. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 30.

40. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 30.

41. (Currently Amended) An electronic device comprising :

a source signal line driver circuit [[,]] ;

a first gate signal line driver circuit [[,]] ;

a second gate signal line driver circuit [[,]] ;

a pixel portion including a plurality of pixels [[,]] ;

a plurality of source signal lines electrically connected to said source signal line driver circuit [[,]] ;

a plurality of first gate signal lines electrically connected to said first gate signal line driver circuit [[,]] ;

a plurality of second gate signal lines electrically connected to said second gate signal line driver circuit [[,]] ; and

a plurality of power supply ~~line~~ lines,

wherein:

at least one of said plurality of pixels ~~each have~~ has a ~~switching~~ first TFT, ~~an EL driving~~ a second TFT, ~~an eliminating~~ a third TFT, and an EL element;

a gate electrode of said ~~switching~~ first TFT is electrically connected to one of said plurality of first gate signal lines;

one of a source region and a drain region of said ~~switching~~ first TFT is electrically connected to one of said plurality of source signal lines, and ~~another thereof~~ the other of the source region and the drain region of the first TFT is electrically connected to a gate electrode of said ~~EL driving~~ second TFT;

a gate electrode of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of second gate signal lines;

one of a source region and a drain region of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the third TFT is electrically connected [[a]] the gate electrode of said ~~EL driving~~ second TFT;

one of a source region and a drain region of said ~~EL driving~~ second TFT is electrically connected to the one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the second TFT is electrically connected to said EL element ;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said entire plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1);

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same;

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$, and

said display periods Tr1, Tr2, ···, Tr(n) appear in a random order.

42. (Original) A device according to claim 41, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

43. (Original) A device according to claim 41, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

44. (Currently Amended) A device according to claim 41, wherein each of said ~~switching~~ first TFT, the ~~EL driving~~ second TFT, and the ~~eliminating~~ third TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

45. (Currently Amended) A device according to claim 41, wherein said ~~EL driving~~ second TFT becomes an OFF state when an electric potential of the one of said power supply line is applied to said gate electrode of said ~~EL driving~~ second TFT.

46. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 41.

47. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 41.

48. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 41.

49. (Currently Amended) An electronic device comprising :

a source signal line driver circuit [[,]] ;

a first gate signal line driver circuit [[,]] ;

a second gate signal line driver circuit [[,]] ;

a pixel portion including a plurality of pixels [[,]] ;

a plurality of source signal lines electrically connected to said source signal line driver circuit [[,]] ;

a plurality of first gate signal lines electrically connected to said first gate signal line driver circuit [[,]] ;

a plurality of second gate signal lines electrically connected to said second gate signal line driver circuit [[,]] ; and

a plurality of power supply ~~line~~ lines ~~held at a constant electric potential~~,

wherein:

at least one of said plurality of pixels ~~each have~~ has a ~~switching~~ first TFT, ~~an EL driving~~ a second TFT, ~~an eliminating~~ a third TFT and an EL element;

said EL element includes a pixel electrode, an opposing electrode ~~held at a constant electric potential,~~ and an EL layer formed between said pixel electrode and opposing electrode;

a gate electrode of said ~~switching~~ first TFT is electrically connected to one of said plurality of first gate signal lines;

one of a source region and a drain region of said ~~switching~~ first TFT is electrically connected to one of said plurality of source signal lines, and ~~another thereof~~ the other of the source region and the drain region of the first TFT is electrically connected to a gate electrode of said ~~EL driving~~ second TFT;

a gate electrode of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of second gate signal lines;

one of a source region and a drain region of said ~~eliminating~~ third TFT is electrically connected to one of said plurality of power supply ~~line~~ lines, and ~~another thereof~~ the other of the source region and the drain region of the third TFT is electrically connected [[a]] the gate electrode of said ~~EL driving~~ second TFT;

a source region and a drain region of said ~~EL driving~~ second TFT~~, wherein one~~ is electrically connected to the one of said plurality of power supply ~~line~~ lines whereas the other of the

source region and the drain region of the second TFT is electrically connected to [[a]] the pixel electrode of said EL element;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1);

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same;

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$; and

said display periods Tr1, Tr2, ···, Tr(n) appear in a random order.

50. (Currently Amended) A device according to claim 49, wherein said EL layer [[is]] comprises at least one of a low molecular organic material [[or]] and a polymer organic material.

51. (Currently Amended) A device according to claim 49, wherein said low molecular organic material ~~is made of~~ comprises at least one of Alq_3 (tris-8-quinolilite-aluminum) [[or]] and TPD (triphenylamine derivative).

52. (Currently Amended) A device according to claim 49, wherein said polymer organic material ~~is made of~~ comprises at least one of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), [[or]] and polycarbonate.

53. (Original) A device according to claim 49, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

54. (Original) A device according to claim 49, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

55. (Currently Amended) A device according to claim 49, wherein each of said ~~switching~~ first TFT, the ~~EL driving~~ second TFT, and the ~~eliminating~~ third TFT ~~are at least one of~~ is selected from an N channel TFT [[or]] and a P channel TFT.

56. (Currently Amended) A device according to claim 49, wherein said ~~EL driving~~ second TFT becomes an OFF state when an electric potential of the one of said plurality of power supply ~~line~~ lines is applied to said gate electrode of said ~~EL driving~~ second TFT.

57. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 49.

58. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 49.

59. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 49.

60. (Currently Amended) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion including a plurality of pixels,

wherein ~~each~~ at least one of the pixels comprises at least a first TFT electrically connected to the first gate signal line driver circuit, and a second TFT electrically connected to the second gate signal line driver circuit,

wherein said plurality of pixels have a plurality of EL elements, and

wherein respective drives of said plurality of EL elements are controlled by a digital data signal outputted from said source signal line driver circuit, a first selecting signal outputted from said first gate signal line driver circuit, and a second selecting signal outputted from said second gate signal line driver circuit.

61. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 60.

62. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 60.

63. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 60.

64. (Currently Amended) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion including a plurality of pixels,

wherein ~~each~~ at least one of the pixels comprises at least a first TFT electrically connected to the first gate signal line driver circuit, and a second TFT electrically connected to the second gate signal line driver circuit,

wherein said plurality of pixels includes a plurality of EL elements; and

wherein a luminescing time of said EL element is controlled by a digital data signal outputted from said source signal line driver circuit, a first selecting signal outputted from said first gate signal line driver circuit, and a second selecting signal outputted from said second gate signal line driver circuit, to thereby perform gray-scale display.

65. (Currently Amended) A computer, which ~~uses~~ comprises said electronic device according to claim 64.

66. (Currently Amended) A video camera, which ~~uses~~ comprises said electronic device according to claim 64.

67. (Currently Amended) A DVD player, which ~~uses~~ comprises said electronic device according to claim 64.

68. (New) An electronic device according to claim 7,

wherein the a first TFT is a switching TFT,

wherein the second TFT is an EL driving TFT, and

wherein the third TFT is an eliminating TFT.

69. (New) An electronic device according to claim 13,

wherein the a first TFT is a switching TFT,

wherein the second TFT is an EL driving TFT, and

wherein the third TFT is an eliminating TFT.

70. (New) An electronic device according to claim 22,

wherein the a first TFT is a switching TFT,

wherein the second TFT is an EL driving TFT, and

wherein the third TFT is an eliminating TFT.

71. (New) An electronic device according to claim 30,

wherein the a first TFT is a switching TFT,

wherein the second TFT is an EL driving TFT, and

wherein the third TFT is an eliminating TFT.

72. (New) An electronic device according to claim 41,

wherein the a first TFT is a switching TFT,

wherein the second TFT is an EL driving TFT, and

wherein the third TFT is an eliminating TFT.

73. (New) An electronic device according to claim 49,

wherein the a first TFT is a switching TFT,

wherein the second TFT is an EL driving TFT, and

wherein the third TFT is an eliminating TFT.

74. (New) An electronic device according to claim 7, further comprising a capacitor between the gate electrode of the second TFT and the one of the plurality of power supply lines.

75. (New) An electronic device according to claim 13, further comprising a capacitor between the gate electrode of the second TFT and the one of the plurality of power supply lines.

76. (New) An electronic device according to claim 30, further comprising a capacitor between the gate electrode of the second TFT and the one of the plurality of power supply lines.

77. (New) An electronic device according to claim 41, further comprising a capacitor between the gate electrode of the second TFT and the one of the plurality of power supply lines.

78. (New) An electronic device according to claim 49, further comprising a capacitor between the gate electrode of the second TFT and the one of the plurality of power supply lines.